WHAT IS CLAIMED IS:

1. A metal-insulator-metal (MIM) capacitor plate, comprising:

a first conductive layer, the first conductive layer comprising a first material;

at least one thin conductive material layer disposed over the first conductive layer, the thin conductive material layer comprising a second material, the second material being different than the first material; and

at least one second conductive layer disposed over at least one of the at least one thin conductive material layers.

2. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive material layer comprises TiN, TaN, or WN.

3. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive material layer comprises a thickness of about 450 Angstroms or less.

4. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive material layer comprises:

a first barrier layer disposed over the first conductive layer; and

a conductive layer disposed over the first barrier layer.

5. The MIM capacitor plate according to Claim 4, wherein the first barrier layer comprises Ti, Ta or W, and wherein the conductive layer comprises TiN, TaN, or WN.

6. The MIM capacitor plate according to Claim 4, wherein the at least one thin conductive material layer further comprises a second barrier layer disposed over the conductive layer.

7. The MIM capacitor plate according to Claim 6, wherein the first barrier layer comprises Ti, Ta or W, wherein the conductive layer comprises TiN, TaN, or WN, and wherein the second barrier layer comprises Ti, Ta or W.

8. The MIM capacitor plate according to Claim 1, wherein the at least one second conductive layer comprises the first material.

9. The MIM capacitor plate according to Claim 1, wherein the first conductive layer and the at least one second conductive layer comprise Al.

10. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate is formed in a metallization layer of a semiconductor device, the metallization layer comprising a plurality of conductive lines having a first thickness, wherein the MIM capacitor plate comprises the first thickness.

11. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate comprises a bottom plate of a MIM capacitor.

12. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate comprises a top plate of a MIM capacitor.

13. A metal-insulator-metal (MIM) capacitor, comprising:

a first plate;

a dielectric material disposed over the first plate; and

a second plate disposed over the dielectric material, wherein the first plate or the second plate comprises:

a first conductive layer, the first conductive layer comprising a first material;

at least one thin conductive material layer disposed over the first conductive layer, the at least one thin conductive material layer comprising a second material, the second material being different than the first material; and

at least one second conductive layer disposed over at least one of the at least one thin conductive material layers.

14. The MIM capacitor according to Claim 13, wherein either the first plate or second plate is formed in a metallization layer of a semiconductor device, the metallization layer comprising a plurality of conductive lines having a first thickness, wherein the MIM capacitor first plate or second plate comprises the first thickness.

15. The MIM capacitor according to Claim 13, wherein the at least one thin conductive material layer comprises TiN, TaN, or WN.

16. The MIM capacitor according to Claim 15, wherein the at least one thin conductive material layer comprises a thickness of about 450 Angstroms or less.

17. The MIM capacitor according to Claim 13, wherein the at least one thin conductive material layer comprises:

a first barrier layer disposed over the first conductive layer; and

a conductive layer disposed over the first barrier layer.

18. The MIM capacitor according to Claim 17, wherein the first barrier layer comprises Ti, Ta or W, and wherein the conductive layer comprises TiN, TaN, or WN.

19. The MIM capacitor according to Claim 17, wherein the at least one thin conductive material layer further comprises a second barrier layer disposed over the conductive layer.

20. The MIM capacitor according to Claim 19, wherein the first barrier layer comprises Ti, Ta or W, wherein the conductive layer comprises TiN, TaN, or WN, and wherein the second barrier layer comprises Ti, Ta or W.

21. The MIM capacitor according to Claim 13, wherein the first conductive layer and the at least one second conductive layer comprise the same material.

22. The MIM capacitor according to Claim 13, wherein the first conductive layer and the at least one second conductive layer comprise Al.

23. The MIM capacitor according to Claim 13, wherein the first plate comprises:

a first conductive layer, the first conductive layer comprising a first material;

at least one first thin conductive material layer disposed over the first conductive layer, the at least one first thin conductive material layer comprising a second material, the second material being different than the first material; and

at least one second conductive layer disposed over at least one of the at least one thin conductive material layers;

and wherein the second plate comprises:

a third conductive layer disposed over the dielectric material, the third conductive layer comprising a third material;

at least one second thin conductive material layer disposed over the third conductive layer, the at least one second thin conductive material layer comprising a fourth material, the fourth material being different than the third material; and

at least one fourth conductive layer disposed over at least one of the at least one second thin conductive material layers.

24. The MIM capacitor according to Claim 23, wherein the first conductive layer, the at least one second conductive layer, the third conductive layer and the at least one fourth conductive layer comprise Al, and wherein the at least one first thin conductive material layer and the at least one second thin conductive material layer comprise about 450 Angstroms or less of TiN, TaN, or WN.

25. The MIM capacitor according to Claim 24, wherein the at least one first thin conductive material layer and the at least one second thin conductive material layer further comprise a barrier layer disposed over or under the TiN, TaN or WN.

26. A semiconductor device, comprising:

a workpiece;

at least one metallization layer formed over the workpiece;

at least one metal-insulator-metal (MIM) capacitor formed over the workpiece, the MIM capacitor comprising a first plate formed within the at least one metallization layer, a dielectric material disposed over the first plate, and a second plate disposed over the dielectric material; and

at least one first conductive line formed in the at least one metallization layer of the semiconductor device, wherein the at least one first conductive line comprises a first thickness, and wherein the MIM capacitor first plate comprises the first thickness.

27. The semiconductor device according to Claim 26, wherein the first plate and the at least one first conductive line comprise:

a first conductive layer, the first conductive layer comprising a first material;

at least one thin conductive material layer disposed over the first conductive layer, the thin conductive material layer comprising a second material, the second material being different than the first material; and

at least one second conductive layer disposed over at least one of the at least one thin conductive material layers.

28. The semiconductor device according to Claim 27, wherein the first conductive layer and the at least one second conductive layer comprise Al, and wherein the at least one thin conductive material layer comprises TiN, TaN, or WN.

29. The semiconductor device according to Claim 27, wherein the at least one thin conductive material layer comprises a first layer of Ti, Ta or W disposed over the first conductive layer, and a second layer of TiN, TaN, or WN disposed over the first layer of Ti, Ta or W.

30. The semiconductor device according to Claim 27, wherein the at least one thin conductive material layer comprises a third layer of Ti, Ta or W disposed over the second layer of TiN, TaN, or WN.

31. The semiconductor device according to Claim 26, wherein the first plate is electrically coupled to at least one first conductive line in the metallization layer.

32. A method of manufacturing a metal-insulator-metal (MIM) capacitor, the method comprising:

providing a workpiece;

depositing a first conductive layer over the workpiece, the first conductive layer comprising a first material;

depositing at least one thin conductive material layer over the first conductive layer, the at least one thin conductive material layer comprising a second material, the second material being different than the first material;

depositing at least one second conductive layer over at least one of the at least one thin conductive material layers; and

patterning the at least one second conductive layer, the at least one thin conductive material layer and the first conductive layer to form a first plate.

33. The method according to Claim 32, further comprising forming a plurality of conductive lines in the at least one second conductive layer, the at least one thin conductive material layer and the first conductive layer simultaneously while forming the first plate, wherein the plurality of conductive lines resides in a metallization layer of a semiconductor device.

34. The method according to Claim 33, wherein patterning the at least one second conductive layer, the at least one thin conductive material layer and the first conductive layer to form the first plate and the plurality of conductive lines comprises using a single mask.

35. The method according to Claim 32, further comprising:

depositing a dielectric material over the first plate;

depositing a third conductive layer over the dielectric material; and

patterning the third conductive layer and the dielectric material to form a MIM capacitor, wherein the patterned third conductive layer comprises a top plate of the MIM capacitor, and wherein the dielectric material comprises a capacitor dielectric of the MIM capacitor.

36. The method according to Claim 32, further comprising, before depositing the first conductive layer over the workpiece:

forming a second plate over the workpiece, the second plate comprising a bottom plate of a MIM capacitor; and

forming a capacitor dielectric over the second plate, wherein the first plate comprises a top plate of the MIM capacitor, and wherein depositing the first conductive layer comprises depositing the first conductive layer over the MIM capacitor.

37. The method according to Claim 32, wherein depositing the at least one thin conductive material layer comprises depositing about 450 Angstroms of material.

38. The method according to Claim 32, wherein depositing the at least one thin conductive material layer comprises depositing TiN, TaN, or WN.

39. The method according to Claim 38, further comprising depositing a barrier layer of Ti, Ta, or W over or beneath the TiN, TaN, or WN.

40. The method according to Claim 32, wherein depositing the first conductive layer and depositing the at least one second conductive layer comprise depositing Al.